## AMENDMENTS TO THE CLAIMS

Please add or amend the claims to read as follows, and cancel without prejudice or disclaimer to resubmission in a divisional or continuation application claims indicated as cancelled:

1. **(Canceled)**

2. **(Currently amended)** ~~The~~ A method ~~of claim 1~~ comprising:

enabling renaming of a source of a particular micro-operation even though two or more pointers – each currently indicating where values of a respective group of bits of said source will be found when said particular micro-operation is executed – do not all point to the same register,

wherein enabling renaming of said source comprises:

generating one or more micro-operations to merge said values into a single register; and

inserting said one or more micro-operations into a sequence of micro-operations that includes said particular micro-operation.

3. **(Original)** The method of claim 2, wherein generating said one or more micro-operations comprises generating two micro-operations when said two or more pointers are three pointers that currently point to three registers, respectively.

4-8 **(Canceled)**

9. **(Currently amended)** ~~The~~ A method ~~of claim 8,~~ comprising:

enabling renaming of sources of micro-operations appearing later in a sequence of micro-operations than a particular micro-operation without having to wait for values of bits of a source of said particular micro-operation to be calculated, even though two or more pointers – each currently indicating where values of a respective group of bits of said source will be found when said particular micro-operation is executed – do not all point to the same register,

wherein enabling renaming of sources of said micro-operations appearing later in said sequence comprises renaming said source of said particular micro-operation, and

wherein renaming said source of said particular micro-operation comprises:

generating one or more new micro-operations to merge said values into a single register; and

inserting said one or more new micro-operations into said sequence.

10-11 **(Canceled)**

12. **(Currently amended)** ~~The~~ A method ~~of claim 11,~~ comprising:

if two or more pointers – each currently indicating where values of a respective group of bits of said source will be found when a particular micro-operation is executed – do not all point to the same register, enabling execution of micro-operations appearing later than said particular micro-operation in a sequence of micro-operations without having to wait for said values to be calculated, if said micro-operations appearing later in said sequence are not dependent upon said source, not dependent upon said values, and not dependent upon a result of said particular micro-operation,

wherein enabling execution of said micro-operations appearing later in said sequence comprises renaming said source of said particular micro-operation, and

wherein renaming said source of said particular micro-operation comprises:

generating one or more new micro-operations to merge said values into a single register; and

inserting said one or more new micro-operations into said sequence.

13. **(Original)** A method comprising:

allocating a first register to store results of a first micro-operation a destination of which is an entire architectural register;

subsequently allocating a second register to store results of a second micro-operation a destination of which is a larger partial register of said architectural register; and

when a third register is about to be allocated to store results of a third micro-operation a destination of which is a smaller partial register contained in said larger partial register, generating a merge micro-operation to merge into a single register a) values stored in said

first register that correspond to bits of said architectural register but not to bits of said larger partial register and b) values stored in said second register that correspond to bits of said larger partial register but not to bits of said smaller partial register, and inserting said merge micro-operation ahead of said third micro-operation into a sequence of micro-operations including at least said first micro-operation, said second micro-operation and said third micro-operation.

14. **(Original)** The method of claim 13, further comprising:

after inserting said merge micro-operation into said sequence, allocating said third register to store said results of said third micro-operation.

15. **(Original)** The method of claim 14, further comprising:

updating pointers to indicate that values that correspond to bits of said architectural register but not to bits of said smaller partial register will be stored in said single register when said merge micro-operation is executed and values that correspond to bits of said smaller partial register will be stored in said third register when said third micro-operation is executed.

16-19 **(Canceled)**

20. **(Currently amended)** ~~The processor of claim 19, further comprising:~~ A processor comprising:

an architectural register;

a register tracking mechanism to maintain pointers that indicate where results of micro-operations that are to be written to said architectural register upon retirement will be stored when said micro-operations are executed; and

a stall detection and micro-operations injection unit a) to identify that said architectural register is a source of a particular micro-operation and that two or more pointers – each to indicate where values of a respective group of bits of said source will be found when said particular micro-operation is executed – do not point to the same register, b) to generate one or more new micro-operations to merge said values into a

single register, and c) to insert said one or more new micro-operations into a sequence of micro-operations that includes said particular micro-operation,

wherein said pointers include a pointer that indicates where results of a most recently allocated micro-operation that writes to all bits of said architectural register upon retirement are to be stored when said micro-operation is executed.

21. **(Currently amended)** ~~The processor of claim 19, further comprising:~~ A processor comprising:

an architectural register;

a register tracking mechanism to maintain pointers that indicate where results of micro-operations that are to be written to said architectural register upon retirement will be stored when said micro-operations are executed; and

a stall detection and micro-operations injection unit a) to identify that a partial register of said architectural register is a source of a particular micro-operation and that two or more pointers – each to indicate where values of a respective group of bits of said source will be found when said particular micro-operation is executed – do not point to the same register, b) to generate a new micro-operation to merge said values into a single register, and c) to insert said new micro-operation into a sequence of micro-operations that includes said particular micro-operation,

wherein said pointers include a pointer that indicates where results of a most recently allocated micro-operation that writes to all bits of said architectural register upon retirement are to be stored when said micro-operation is executed.

22-25 **(Canceled)**

26. **(Currently amended)** ~~The~~ An apparatus ~~of claim 25, wherein said processor further comprises~~ comprising:

a voltage monitor; and

a processor including at least:

an architectural register;

a register tracking mechanism to maintain pointers that indicate where results of micro-operations, that are to be written to said architectural register upon retirement, will be stored when said micro-operations are executed; and

a stall detection and micro-operations injection unit a) to identify that said architectural register is a source of a particular micro-operation and that two or more pointers – each to indicate where values of a respective group of bits of said source will be found when said particular micro-operation is executed – do not point to the same register, b) to generate one or more new micro-operations to merge said values into a single register, and c) to insert said one or more new micro-operations into a sequence of micro-operations that includes said particular micro-operation,

wherein said pointers include a pointer that indicates where results of a most recently allocated micro-operation that writes to all bits of said architectural register upon retirement will be stored when said micro-operation is executed.

27. **(Currently amended)** ~~The~~ An apparatus ~~of claim 25, wherein said processor further comprises~~ comprising:

a voltage monitor; and

a processor including at least:

an architectural register;

a register tracking mechanism to maintain pointers that indicate where results of micro-operations, that are to be written to said architectural register upon retirement, will be stored when said micro-operations are executed; and

a stall detection and micro-operations injection unit a) to identify that a partial register of said architectural register is a source of a particular micro-operation having a source including a lower portion of bits of said architectural register and that two or more pointers – each to indicate where values of a respective group of bits of said source will be found when said particular micro-operation is executed – do not point to the same register, b) to generate a new micro-operation to merge said values into a single register, and c) to insert said new micro-operation into a sequence of micro-operations that includes said particular micro-operation,

wherein said pointers include a pointer that indicates where results of a most recently allocated micro-operation that writes to all bits of said architectural register upon retirement will be stored when said micro-operation is executed.

28-30 **(Canceled)**

31. **(Currently amended)** ~~An article comprising a storage medium~~ A machine-readable medium having stored thereon instructions, which when executed by a machine, cause the machine to perform a method comprising:

enabling renaming of a source of a particular micro-operation even though two or more pointers – each currently indicating where values of a respective group of bits of said source will be found when said particular micro-operation is executed – do not all point to the same register,

wherein enabling renaming of said source comprises:

generating and inserting into a sequence of micro-operations one or more new micro-operations that merge values distributed among more than one register into a single register.

32. **(Canceled)**

33. **(Currently amended)** The ~~article~~ machine-readable medium of claim 31, wherein generating said one or more new micro-operations comprises generating two micro-operations when said values are distributed among three different registers.

34. **(Canceled)**

35. **(Currently amended)** ~~The processor of claim 34,~~ A processor comprising:

an instruction decoder to decode a macroinstruction into one or more micro-operations; and

means for enabling renaming of a source of a particular micro-operation even though two or more pointers – each currently indicating where values of a respective group of

bits of said source will be found when said particular micro-operation is executed – do not all point to the same register,

wherein said means for enabling comprises:

means for generating one or more micro-operations to merge said values into a single register; and

means for inserting said one or more micro-operations into a sequence of micro-operations that includes said particular micro-operation.

36. **(Original)** The processor of claim 35, wherein said means for generating comprises means for generating two micro-operations when said two or more pointers are three pointers that currently point to three registers, respectively.